REMARKS

The Examiner's Action mailed on October 5, 2004, has been received and its contents carefully considered.

In this Amendment, Applicants have amended independent claim 6 to include the subject matter of dependent claim 9, and have canceled claim 9. Claims 1 and 6 are the independent claims. Claims 1-8 and 10 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner's Action has rejected claims 1-3, 5-7 and 9-10 as being anticipated by *Yonehara et al.* (USP 5,530,266). Because claim 9 has been canceled and the subject matter recited therein amended into independent claim 6, Applicants will treat this rejection as pertaining only to claims 1-3, 5-7 and 10. It is submitted that these claims are patentably distinguishable over this reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 U.S.C. § 102 only if all the features and all the relationships recited in the claim are taught by the referenced structure either by clear disclosure or under the principle of inherency.

Applicants' independent claim 1 is directed to a semiconductor device that includes, *inter alia*, an SOI layer formed on top of an insulation layer, which is disposed on top of a support substrate. The support substrate has at least one groove formed therein which is disposed below a target element whose dielectric

loss is to be controlled. Applicants' independent claim 6 recites similar features, but recites an analog element instead of a target element. By forming the groove in the substrate under the target or analog element, dielectric loss of the overlying element is reduced. This claimed invention is not disclosed by the cited reference.

Yonehara et al. disclose a substrate 44, 61, having a groove disposed below an electronic device 47, 57. However, these grooves are only disclosed as being provided for imparting transparency or transmissivity to the substrate. There is no disclosure from this reference that these grooves are for controlling a dielectric loss of the element, as recited by Applicants' independent clams 1 and 6. Moreover, it is noted that the grooves of *Yonehara et al.* are formed in the substrate regardless of the location of the element, be it analog or not. Thus, not only does this reference not disclose a groove being located below a target or analog element to control its dielectric loss, but this reference does not even suggest this claimed recitation. Instead, *Yonehara et al.* only teach making the substrate thin to give transmissivity to the substrate. Thus, one skilled in the art would have had no motivation from the *Yonehara et al.* disclosure to control a dielectric loss of a target or analog element. As such, it is submitted that Applicants' independent claims 1 and 6, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited reference. It is thus requested that these claims be allowed and that this rejection be withdrawn.

The Examiner's Action has also rejected claims 4 and 8 as being obvious over *Yonehara et al.* in view of *Eda et al.* (USP 5,668,057). It is submitted that these claims are *prima facie* patentably distinguishable over the cited combination of references for at least the following reasons.

Claims 4 and 8 depend from independent claims 1 and 6, respectively. Moreover, *Eda et al.* do not overcome the above noted deficiencies of *Yonehara et al.* Instead, *Eda et al.* only teach a substrate 1 having grooves disposed below a resonator 2, such as shown in Figure 6. The semiconductor of *Eda et al.* does not have an SOI layer disposed over a substrate via an insulation layer, and does not disclose or suggest controlling a dielectric loss of a target or analog element due to the formation of a groove, as recited by Applicants' independent claims 1 and 6. In fact, the control of dielectric loss of a particular element is not even disclosed or suggested by *Eda et al.* Although the semiconductor of *Eda et al.* has an inductance 5, no groove is formed in the substrate below the inductance 5. This clearly shows that *Eda et al.* do not intend to control the dielectric loss of the inductance 5. As such, it is submitted that Applicants' independent claims 4 and 8 are *prima facie* patentably distinguishable over the cited combination of references. It is thus requested that these claims be allowed and it is further requested that these rejections be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would be helpful in expediting the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

February 7, 2005
Date

Robert H. Berdo, Jr.
Registration No. 38,075
RABIN & BERDO, PC
Customer No. 23995
Telephone: 202-371-8976
Facsimile: 202-408-0924

RHB:vm